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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN, VA 22102

EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/433,705	YAMAZAKI, SHUNPEI	
	Examin r	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cov r she t with th corr spondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-17 and 46-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-17,51-69,71-75 and 77-82* is/are rejected.

7)☒ Claim(s) *46-50,70 and 76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *16 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application (PTO-152)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) ☐ Other: .

1. The disclosure is objected to because of the following informalities:

It is believed that regions 316 to 319, 326 and 327 are undoped regions in fig. 12A. It is unclear why regions 316 to 319, 326 and 327 are n^- - type impurity regions (page 26, lines 21-22). The reference numerals should refer to the shaded regions instead of the unshaded regions.

It is believed that regions 334 and 335 are undoped regions in fig. 12A. It is unclear why regions 334 and 335 are n^- - type impurity regions (page 27, line 7). The reference numerals should refer to the shaded regions instead of the unshaded regions.

Appropriate correction is required.

2. Claims 13-17, 46-54, 69-71, 75, 76 and 82 are objected to because of the following informalities: Claim 13, lines 6-7, the phrase "at least one of said first thin film transistor" is unclear whether it is being referred to "said at least one first thin film transistor". Claim 46, line 8, the phrase "at least one of said second n-channel thin film transistor" is unclear whether it is being referred to "said at least one second n-channel thin film transistor"; line 25, the phrase "at least one of said third p-channel thin film transistor" is unclear whether it is being referred to "said at least one third p-channel thin film transistor". Claim 51, lines 6-7, the phrase "at least one of said second thin film transistor" is unclear whether it is being referred to "said at least one second thin film transistor". Appropriate correction is required.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13, 15-17, 51, 53-55, 57-60, 62-64, 66-69, 71-74, 81 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. (Japanese patent application no. 06-148685) in view of Kurokawa.

In regards to claims 13, 51, 69 and 71, Nakazono et al. disclose a semiconductor device in figs. 1-3. It is a liquid crystal display device, comprising: at least one first thin film transistor (TFT) (the TFT on left side of fig. 2) formed over a substrate [1]; a pixel electrode [11] electrically connected to the first thin film transistor; a driver circuit including at least one second thin film transistor (the TFT on right side of fig. 2) formed over the substrate [1] for driving the at least one first thin film transistor, each of the first and second thin film transistors comprising: a semiconductor island [2] on an insulating surface [1]; source and drain regions [7a] formed in the semiconductor island; a channel region [7c] in the semiconductor island between the source and drain regions [7a]; a pair of lightly doped regions [7b] formed between the channel region [7c] and the source and drain regions [7a] wherein an impurity concentration in the lightly doped regions [7b] is smaller than that in the source and drain regions [7a]; a gate electrode [4, 5] formed over the semiconductor island with a gate insulating film [3] interposed therebetween wherein said gate electrode [4, 5] comprises at least a first conductive layer [4] and a second conductive layer [5] formed on the first conductive layer [4].

Nakazono et al. differs from the claimed invention by not showing each of the first and second thin film transistors comprises the first conductive layer having a pair of tapered portions, which extend beyond side edges of the second conductive layer. In

addition, the pair of lightly doped regions has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer, and a pair of second portions, which extend beyond side edges of the first conductive layer, and wherein the impurity concentration in the pair of first portions is smaller than the impurity concentration in the pair of second portions.

Kurokawa shows a semiconductor device comprising a gate electrode [33] having a first conductive layer [31] having a pair of tapered portions, which extend beyond side edges of the second conductive layer [32] in fig. 2. In addition, a pair of lightly doped regions [25] has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer [31], and a pair of second portions, which extend beyond side edges of the first conductive layer [31]. Since the pair of lightly doped regions [25] are formed by ion-implantation and then by diffusion, the impurity concentration at the bottom portion of each of the first portions of regions [25] would be smaller than the impurity concentration at the middle portion of each of the second portions of regions [25].

Since both Nakazono et al. and Kurokawa teach an insulated gate electrode having two conductive layers and a pair of lightly doped regions, it would have been obvious to have the gate electrode structure and the lightly doped regions of Kurokawa in each of the thin film transistors of Nakazono et al. because they prolong the life of the transistor and restrain the short channel effect.

It is inherent that the semiconductor device is an active matrix display device because it comprises a TFT array.

In regards to claims 55, 60, 64, 72-74, Nakazono et al. disclose a semiconductor device in figs. 1-3. It is a liquid crystal display device, comprising: at least one first thin film transistor (TFT) (the TFT on left side of fig. 2) formed over a substrate [1]; a pixel electrode [11] electrically connected to the first thin film transistor; a driver circuit including at least one second thin film transistor (the TFT on right side of fig. 2) formed over the substrate [1] for driving the at least one first thin film transistor, each of the first and second thin film transistors comprising: a semiconductor island [2] on an insulating surface [1]; source and drain regions [7a] formed in the semiconductor island; a channel region [7c] in the semiconductor island between the source and drain regions [7a]; a pair of lightly doped regions [7b] formed between the channel region [7c] and the source and drain regions [7a] wherein an impurity concentration in the lightly doped regions [7b] is smaller than that in the source and drain regions [7a]; a gate electrode [4, 5] formed over the semiconductor island with a gate insulating film [3] interposed therebetween wherein said gate electrode [4, 5] comprises at least a first conductive layer [4] and a second conductive layer [5] formed on the first conductive layer [4].

Nakazono et al. differs from the claimed invention by not showing each of the first and second thin film transistors comprises the first conductive layer having a pair of tapered portions, which extend beyond side edges of the second conductive layer. In addition, the pair of lightly doped regions has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer, and a pair of second portions, which extend beyond side edges of the first conductive layer, and the

concentration of the impurity in the pair of first portions monotonically increases in a direction from the channel region toward the source and drain regions.

Kurokawa shows a semiconductor device comprising a gate electrode [33] having a first conductive layer [31] having a pair of tapered portions, which extend beyond side edges of the second conductive layer [32] in fig. 2. In addition, a pair of lightly doped regions [25] has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer [31], and a pair of second portions, which extend beyond side edges of the first conductive layer [31]. Since the pair of lightly doped regions [25] are formed by ion-implantation and then by diffusion, the impurity concentration at the bottom portion of each of the first portions of regions [25] would be smaller than the impurity concentration at the middle portion of each of the second portions of regions [25] in a direction from the channel region toward the source and drain regions. Therefore, it is inherent that the impurity concentration at the bottom portion of each of the first portions of regions [25] monotonically increases toward the middle portion of each of the second portions of regions [25] in a direction from the channel region toward the source and drain regions.

Since both Nakazono et al. and Kurokawa teach an insulated gate electrode having two conductive layers and a pair of lightly doped regions, it would have been obvious to have the gate electrode structure and the lightly doped regions of Kurokawa in each of the thin film transistors of Nakazono et al. because they prolong the life of the transistor and restrain the short channel effect.

It is inherent that the semiconductor device is an active matrix display device because it comprises a TFT array.

In regards to claims 15, 53, 57, 66, 81, the combined device further discloses the semiconductor island is a crystalline silicon island.

In regards to claims 16, 54, 58, 62, 67, the combined device further discloses the first conductive layer includes an n-type silicon containing phosphorus and the second conductive layer includes tungsten silicide.

In regards to claims 17, 59, 63, 68, 82, the combined device of Nakazono et al. and Kurokawa further discloses the liquid crystal display can be used in a rear-type projector (a liquid crystal television) (page 5, lines15-18 of the English translation of Nakazono et al.).

5. Claims 14, 52, 56, 61, 65, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. in view Kurokawa, further in view of Maddox, III.

In regards to claims 14, 52, 56, 61 and 65, Nakazono et al. and Kurokawa differ from the claimed invention by not showing an angle between the tapered portions of the first conductive layer and the gate insulating film is in a range of 3 to 60 degrees.

Maddox, III discloses an angle between the tapered portions of the gate electrode and the gate insulating film is less than 60 degrees in fig. 2.

Since both Kurokawa and Maddox, III teach an insulated gate transistor having a tapered gate electrode, it would have been obvious to have the tapered gate electrode of Maddox, III in Kurokawa because it minimizes the problem of punchthrough in the thin film transistor.

6. Claims 75 and 77-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. in view of Kurokawa, further in view of Hamada.

In regards to claims 75 and 77-80, Nakazono et al. and Kurokawa differ from the claimed invention by not showing the active matrix display device is an electroluminescent display device.

Hamada discloses an active matrix display device is an electroluminescent display device [201] in fig. 8.

Since both Nakazono et al. and Hamada teach a display device includes a thin film transistor as a switching element, it would have been obvious to have the electroluminescent display element of Hamada to replace the liquid crystal element of Nakazono et al. because it provides a much clear image than liquid crystal.

5. Applicant's arguments filed 6/16/03 have been fully considered but they are not persuasive.

It is noted, in page 9 of the remarks, that the Applicant is still awaits consideration of the Information Disclosure Statement (IDS) filed January 3, 2001. However, the Examiner did not receive any IDS filed on 1/3/01. The Examiner requests the Applicant send him another copy of the IDS filed on 1/3/01.

It is urged, in pages 9-10 of the remarks, that regions 316 to 319, 326, 327, 334 and 335 are formed as low concentration impurity regions. However, the arrows of the above reference numerals are not pointing to the low concentration impurity regions in the figures. It is requested that the Applicant correct the figures so that the arrows of the above reference numerals are pointing to the low concentration impurity regions.

It is urged, in page 11 of the remarks, that Nakazono and Kurokawa do not teach or suggest the impurity concentration in the pair of first portions overlapping with the first conductive layer of the gate electrode is smaller than the impurity concentration in the pair of second portions outside the first conductive layer of the gate electrode in at least one of the first TFTs connected to the pixel electrode. However as mentioned in the rejection, Kurokawa discloses the impurity concentration of the bottom portion of each of first portions of regions [25] overlapping with the first conductive layer of the gate electrode is smaller than the impurity concentration of the middle portion of each of the second portions of regions [25] outside the first conductive layer of the gate electrode. The combined device of Nakazono and Kurokawa teaches the impurity concentration in the pair of first portions overlapping with the first conductive layer of the gate electrode is smaller than the impurity concentration in the pair of second portions outside the first conductive layer of the gate electrode in at least one first TFT connected to the pixel electrode.

It is urged, in page 12 of the remarks, that Nakazono and Kurokawa do not teach or suggest the impurity concentration in the pair of first portions overlapping with the first conductive layer of the gate electrode is smaller than the impurity concentration in the pair of second portions outside the first conductive layer of the gate electrode in at least one of the second TFTs in the driver circuit. However as mentioned in the rejection, Kurokawa discloses the impurity concentration of the bottom portion of each of first portions of regions [25] overlapping with the first conductive layer of the gate electrode is smaller than the impurity concentration of the middle portion of each of the second

portions of regions [25] outside the first conductive layer of the gate electrode. The combined device of Nakazono and Kurokawa teaches the impurity concentration in the pair of first portions overlapping with the first conductive layer of the gate electrode is smaller than the impurity concentration in the pair of second portions outside the first conductive layer of the gate electrode in at least one second TFT in the driver circuit.

It is urged, in page 12 of the remarks, that the Official Action does not provide a basis in fact and/or technical reasoning to reasonably support the determination that the concentration of the impurity in the pair of first portions in Nakazono monotonically increases in a direction from the channel forming region toward the source and drain regions. Since the pair of lightly doped regions [25] are formed by ion-implantation and then by diffusion, the impurity concentration at the bottom portion of each of the first portions of regions [25] would be smaller than the impurity concentration at the middle portion of each of the second portions of regions [25] in a direction from the channel region toward the source and drain regions. Therefore, Nakazono inherently shows the impurity concentration at the bottom portion of each of the first portions of regions [25] monotonically increases toward the middle portion of each of the second portions of regions [25] in a direction from the channel region toward the source and drain regions.

Therefore, the combined device of Nakazono et al. and Kurokawa, the combined device of Nakazono et al., Kurokawa and Maddox, and the combined device of Nakazono et al., Kurokawa and Hamada show all the elements of the claimed invention.

6. Claim 46 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

7. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claims not found in the prior art of record is a driver circuit comprises a p-channel thin film transistor having a gate electrode comprises at least a third conductive layer and a fourth conductive layer formed on the third conductive layer, wherein side edges of the third conductive layer are coextensive with side edges of the fourth conductive layer.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
September 7, 2003

Steven Loke